

Abstract

Evaluation circuit and method for detecting and/or locating faulty data words in a data stream T_n

The evaluation circuit according to the invention comprises a first linear automaton circuit (L_1) and also a second linear automaton circuit (L_2) connected in parallel, each having a set of states $z(t)$, which have a common input line for receiving a data stream T_n . The first linear automaton circuit (L_1) and the second linear automaton circuit (L_2) are designed such that a first signature (S_1) and a second signature (S_2), respectively, can be calculated. Situated downstream of the two linear automaton circuits (L_1, L_2) are respectively a first logic combination gate (XOR_{L_1}) and a second logic combination gate (XOR_{L_2}), which compare the signature (S_1, S_2) respectively calculated by the linear automaton circuit (L_1, L_2) with a predetermined good signature and output a comparison value.

[Figure 5]